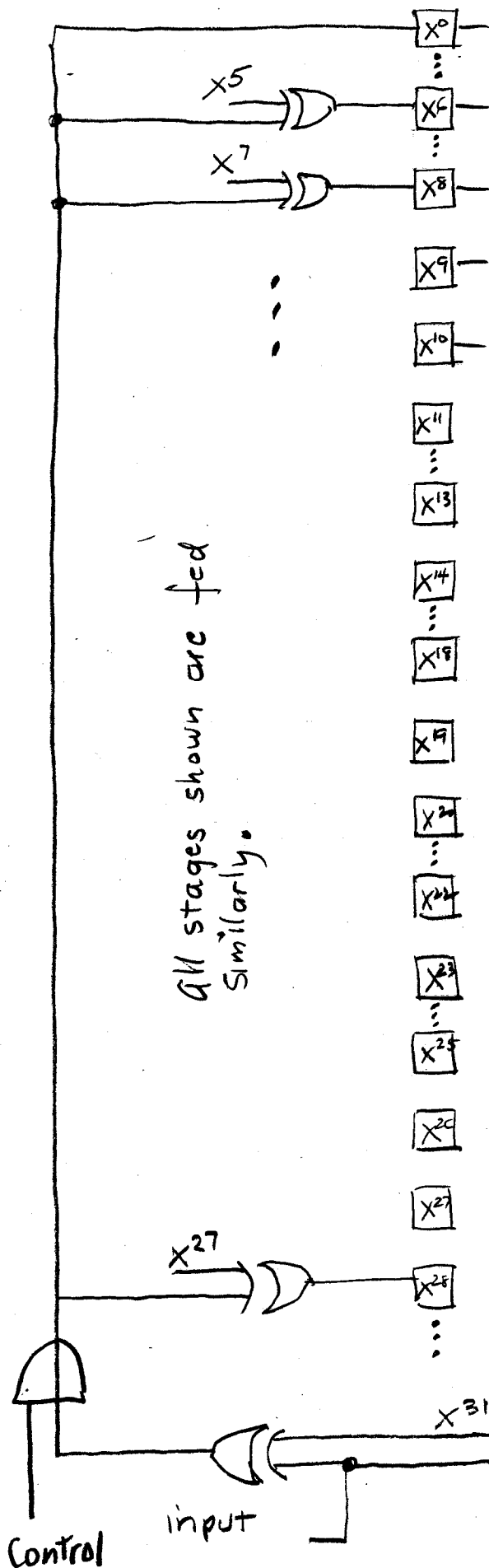


Serial implementation of iscsi poly $G(x)$



1. All stages are D-flops
2. All stages not shown are fed directly (no XOR) from preceding stage.
3. This circuit multiplies the input poly by x^{32} and divides by $G(x)$
4. When the last bit of the dividend has been processed the register stages contain the remainder of the division
5. Control is high for duration of input message. Control is low as complement of remainder shifts out.

